SEMICONDUCTOR DEVICES HAVING DUAL CAPPING LAYER PATTERNS AND METHODS OF MANUFACTURING THE SAME

ABSTRACT OF THE DISCLOSURE

Some embodiments provide a semiconductor substrate having a cell array region and a peripheral circuit region. A plurality of word line patterns are placed in the cell array region, each of which include a word line and a word line capping layer pattern stacked thereon. At least one gate pattern including a gate electrode and a gate capping layer pattern is formed in the peripheral circuit region, the gate capping layer pattern and the word line capping layer pattern having different etching selectivity ratios. A pad interlayer insulating layer and a bit line interlayer insulating layer having approximately the same etching selectivity ratio as the gate capping layer pattern are sequentially formed over a surface of the semiconductor substrate having the gate spacers.